Application No.: 10/811,509 14 Attorney Docket No.: 543822004300

## **AMENDMENTS TO THE DRAWINGS**

The attached sheet(s) of drawings includes changes to Figures 4A-4D.

Attachment:

Replacement sheets (3)

## **REMARKS**

The Examiner has objected to drawing Figures 4A-4D because they do not include the legend –Prior Art--. In accordance with the Examiner's suggestion, Applicants have amended Figures 4A-4D to include the legend –Prior Art--. Accordingly, this objection should be withdrawn.

The Examiner has objected to the Abstract as containing more than 150 words. Applicants have amended the specification to contain fewer than 150 words. Accordingly, this objection should be withdrawn.

Claims 2, 13 and 14 have been amended to place the claims in independent form.

Claims 2-14 stand rejected under 35 USC 112, second paragraph, because step F2 in claim 2 and step H in claim 1 both recited removing the uncovered insulator layer from between the gate electrodes. Claim 2 has been amended to specify in step D) that material plugs are formed on the sacrificial layers for defining a first set of contact openings. In step F2 the insulator layer is removed between a "second set" of mutually adjacent gate electrode tracks. This leaves the insulator layer in between the "first set" of mutually adjacent gate electrode tracks. The insulator layer is then removed in between the "first set" of mutually adjacent gate electrode tracks in step H. This process is shown in Fig. 1H, in which the insulator layer still exists below plug 5, but is removed in the unplugged regions. In Figure 1L, the insulator layer is removed from below where the plug was placed.

Claims 1-5, 8, 10, 11 and 16 stand rejected under 35 USC 102(b) as being anticipated by Doan. This rejection is respectfully traversed. Claim 1 has been cancelled. As stated above, claim 2 has been amended to place this claim in independent form.

Claim 2 that step F includes: F2) removing the uncovered insulator layer on the semiconductor surface between a second set of mutually adjacent gate electrode tracks; F3) producing dopings in predetermined regions of the uncovered semiconductor surface between the mutually adjacent gate electrode tracks for forming the selection transistors; and F4) producing a

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liner layer, which includes silicon nitride. As shown in Figures 2G and 2H and as described in Column 7, lines 17-29, Doan fails to describe any of these claimed steps. Accordingly, claim 2 should be allowed. Claims3-5, 8, 10 and 11, which depend from claim 2 are allowable for at least the same reason. Claim 16 will be discussed below with respect to claim 13, from which it now depends.

Claims 6, 7, 9, 12, 13, 17 and 18 stand rejected under 35 USC 103(a) as being unpatentable over Doan and further in view of Thakar.

Claims 6, 7, 9 and 12, have been amended to depend from claim 2. As explained above, Doan fails to disclose all of the steps claimed in claim 2. Further, Thakar fails to disclose these steps as well. Accordingly, the rejection of claims 6, 7, 9 and 12, should be withdrawn.

Claim 13 has been amended to place the claim in independent form. Claim 13 specifies in step D1' that a hard mask layer is deposited on the sacrificial layer before depositing a resist layer on the hard mask layer. In comparison, Doan describes providing the photoresist layer directly on the sacrificial layer (see Figure 2D and column 6, lines 53 to 57).

Thakar teaches a double-layered structure between a silicon dioxide layer and a resist layer. The double-layered structure may be used as a hard mask as shown in Figure 4. However, Thakar does not teach depositing the hard mask on the sacrificial layer as claimed. Moreover, Thakar does not teach the use of said hard mask structured as a metal block on the sacrificial layer for defining contact openings between the mutual adjacent gate electrode stacks as in claim 13. Furthermore, since neither Doan nor Thakar teaches the advantage achievable by such a hard mask on the sacrificial layer, i.e. the possibility of an inverse formation of the metal blocks as discussed in detail on page 9, line 7 to page 10, line 18 of the present application, forming the claimed hard mask would not be obvious. Since Doan and Thakar fail to disclose the claimed hard mask, claim 13, should be allowed. Claim 17 and 18, which depend from claim 13, should be allowed for at least the same reasons.

Claims 19-23 and 26-30 stand rejected under 35 USC 103(a) as being unpatentable over Doan in view of Thakar. This rejection is respectfully traversed.

According to claims 19 and 23, a second sacrificial layer made of a hard mask layer is formed on the first sacrificial layer in step C3. As discussed above, Neither Doan nor Thakar

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teaches depositing two sacrificial layers. Accordingly, claims 19 and 23 should be allowed. Claims 20-22, and 26-30, which depend from claims 19 and 23, should be allowed for at least the same reasons.

Claims 14 has been rewritten in independent form.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing Attorney Docker No. 543822004300. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: June 27, 2005

Jonathan Bockman

Respectfully subsected.

Registration No.: 45,640 MORRISON & FOERSTER LLP 1650 Tysons Blvd, Suite 300 McLean, Virginia 22102 (703) 760-7769

Attachments